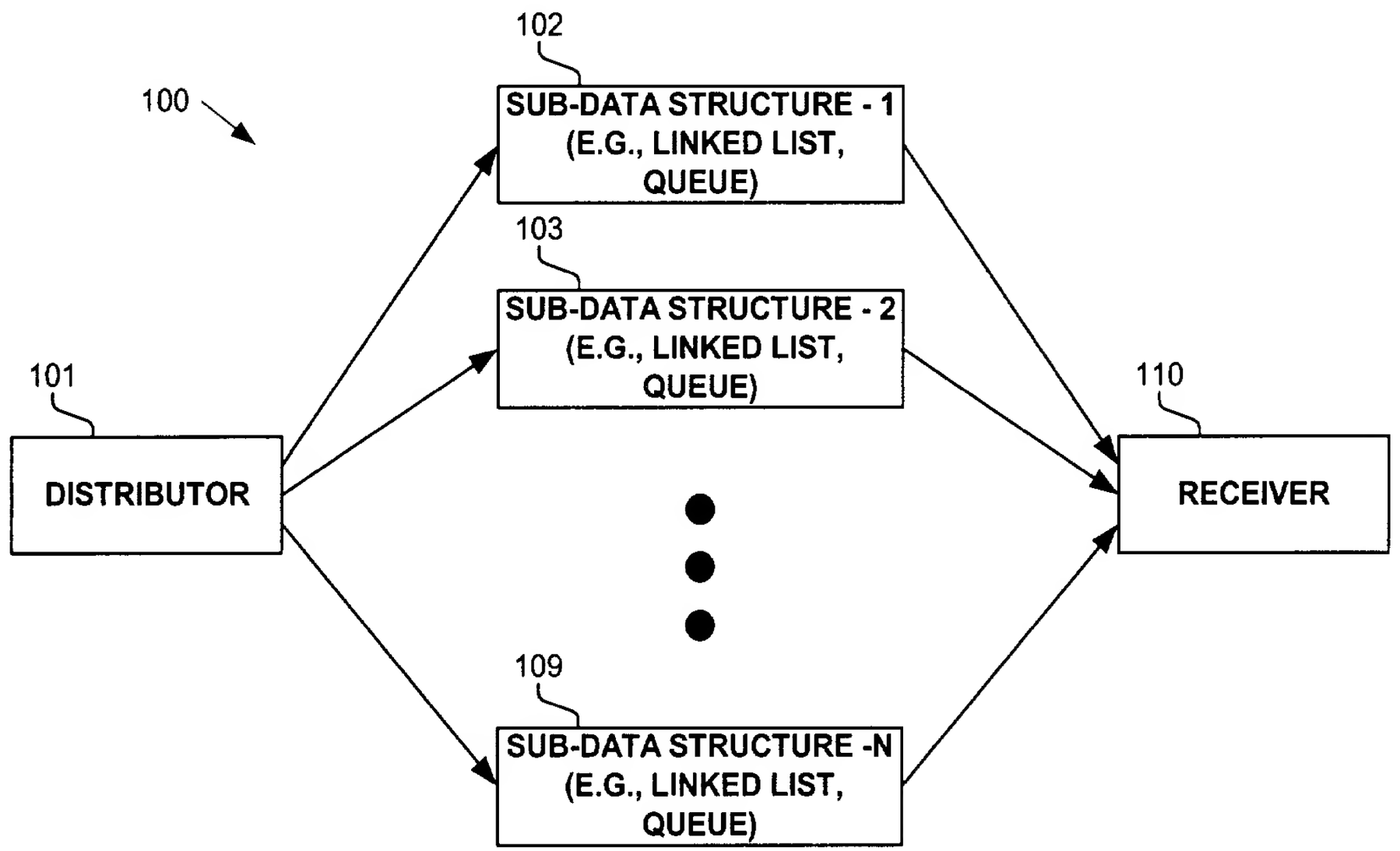
100
102
SUB-DATA STRUCTURE - 1
(E.G., LINKED LIST,
QUEUE)
103
SUB-DATA STRUCTURE - 2
(E.G., LINKED LIST,
QUEUE)
101
DISTRIBUTOR
110
RECEIVER
109
SUB-DATA STRUCTURE -N
(E.G., LINKED LIST,
QUEUE)

FIGURE 1A

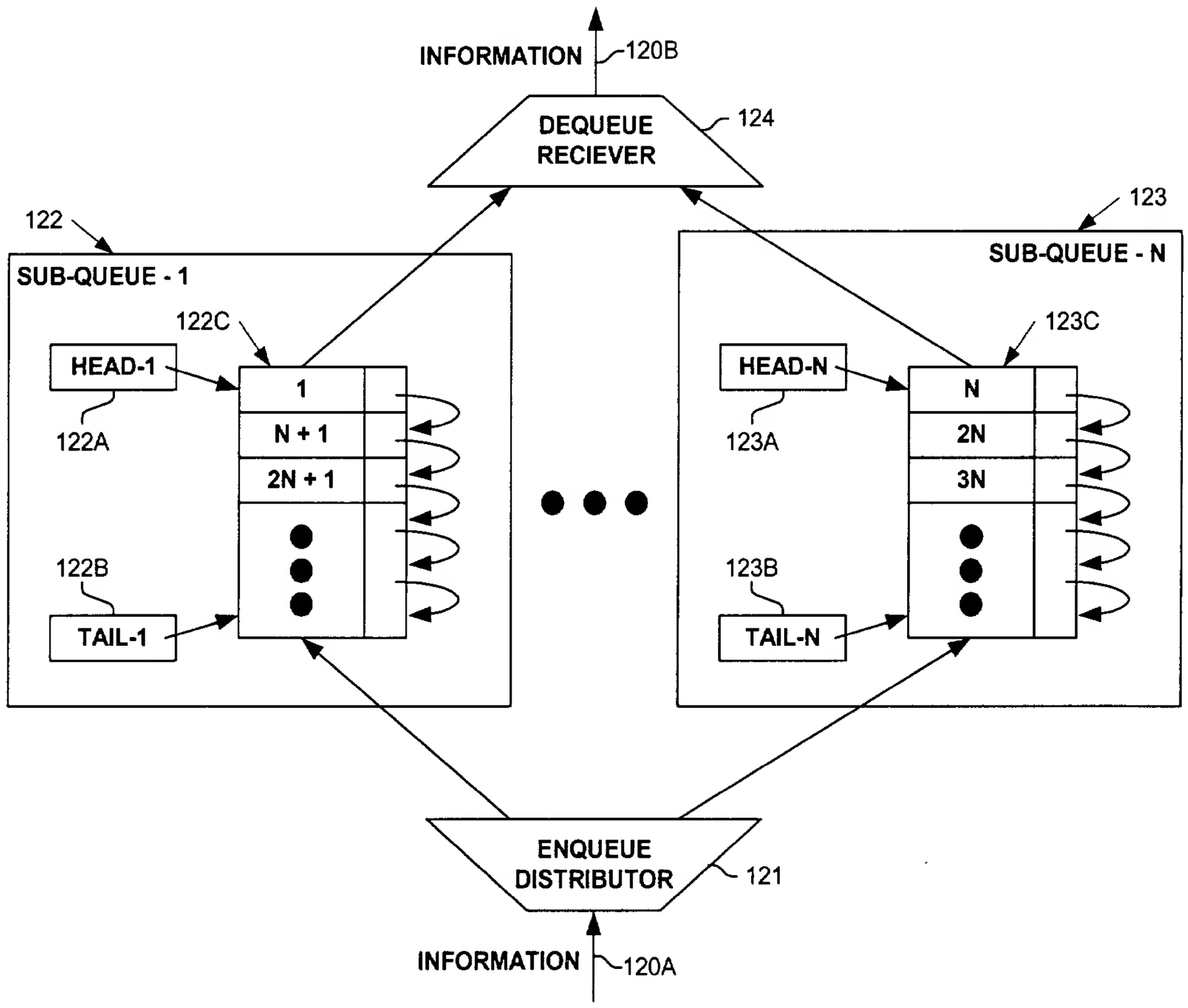
INFORMATION
120B
DEQUEUE
RECIEVER
124
122
SUB-QUEUE - 1
122C
HEAD-1
122A
1
N + 1
2N + 1
122B
TAIL-1
123
SUB-QUEUE - N
123C
HEAD-N
123A
N
2N
3N
123B
TAIL-N
ENQUEUE
DISTRIBUTOR
121
INFORMATION
120A

FIGURE 1B

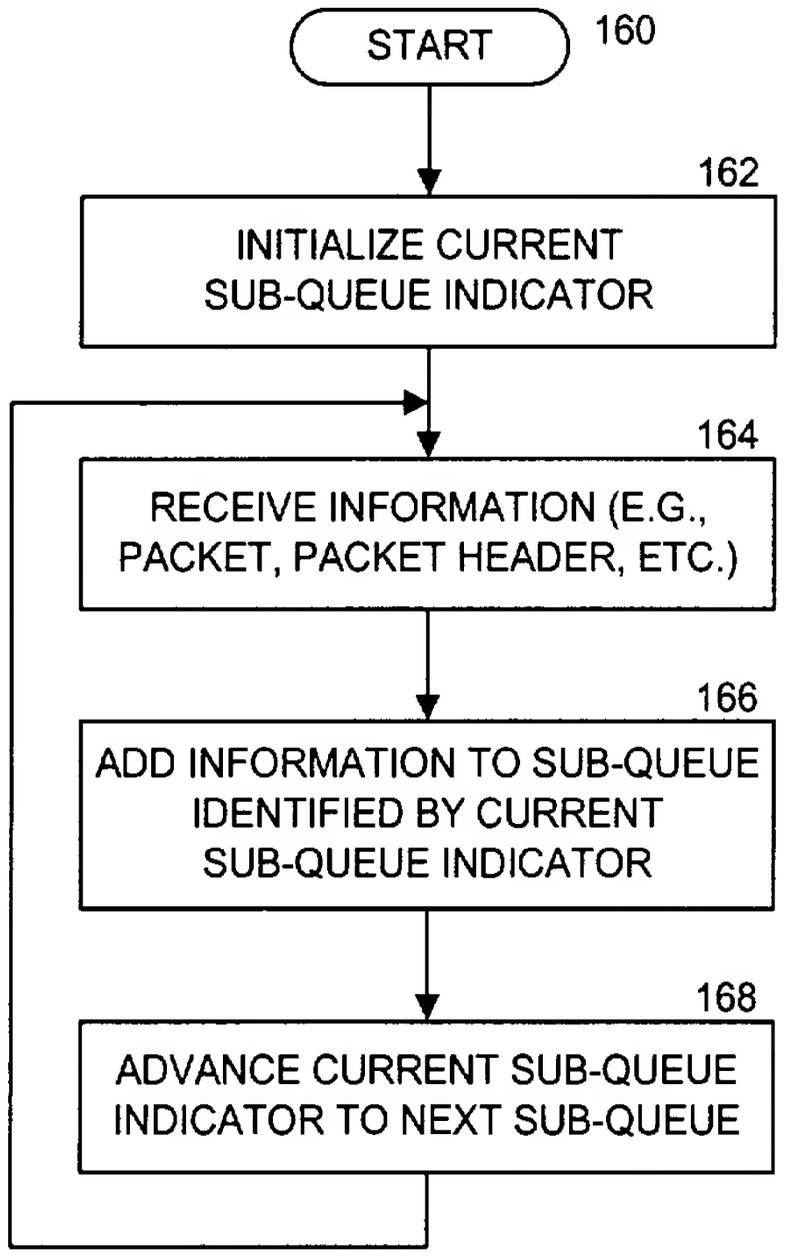

FIGURE 1C

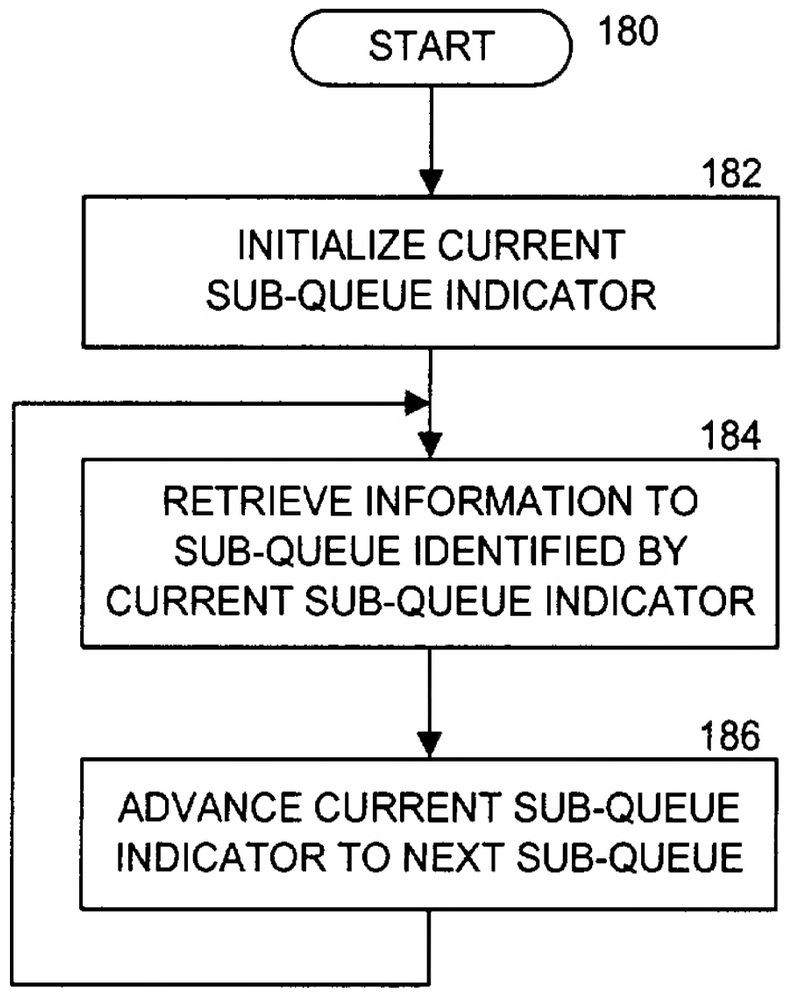

FIGURE 1D

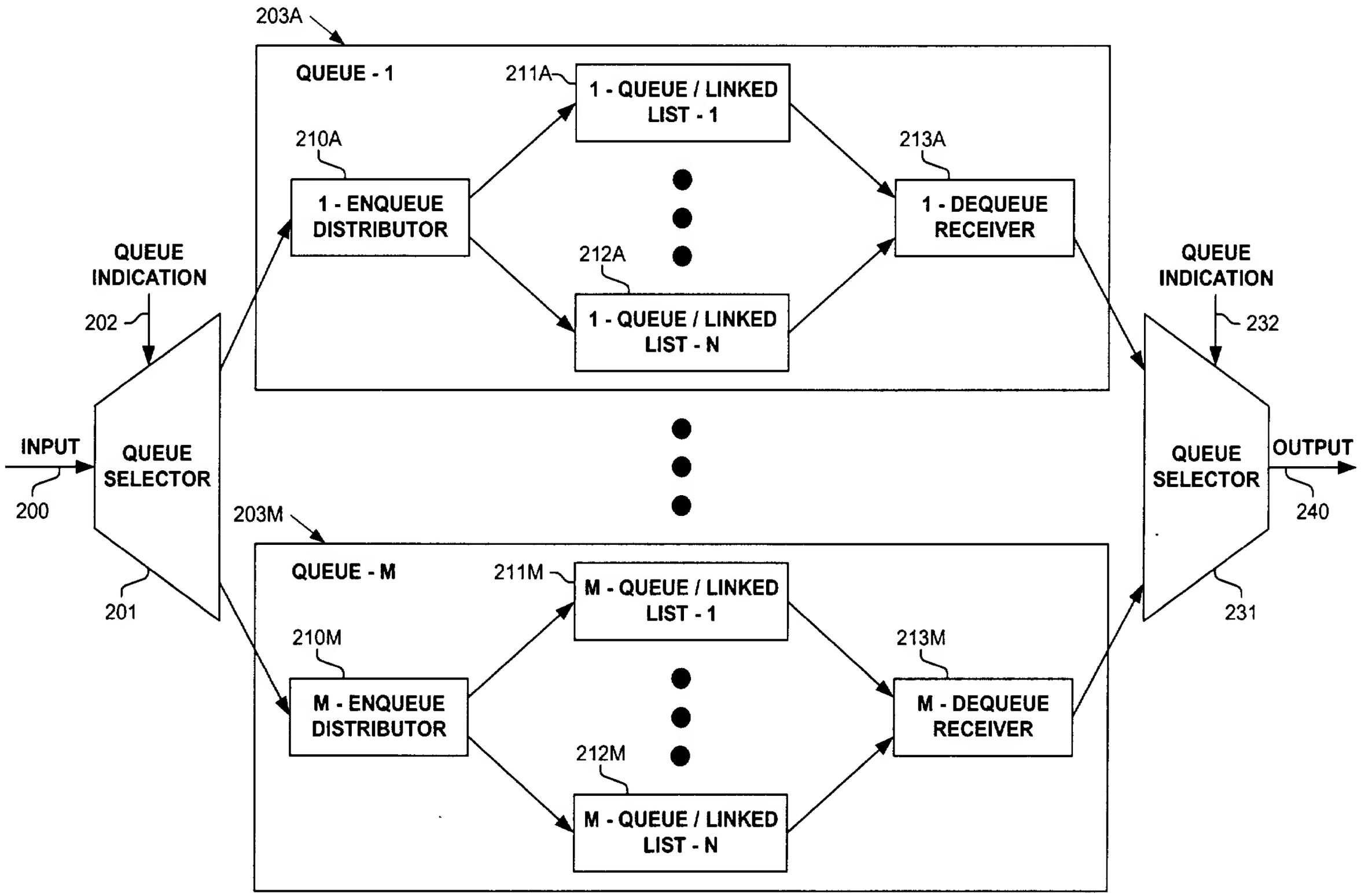
203A
QUEUE - 1
211A
1 - QUEUE / LINKED LIST - 1
210A
213A
1 - ENQUEUE DISTRIBUTOR
1 - DEQUEUE RECEIVER
212A
1 - QUEUE / LINKED LIST - N
QUEUE INDICATION
202
QUEUE INDICATION
232
INPUT
200
QUEUE SELECTOR
QUEUE SELECTOR
OUTPUT
240
201
231
203M
QUEUE - M
211M
M - QUEUE / LINKED LIST - 1
210M
213M
M - ENQUEUE DISTRIBUTOR
M - DEQUEUE RECEIVER
212M
M - QUEUE / LINKED LIST - N

FIGURE 2A

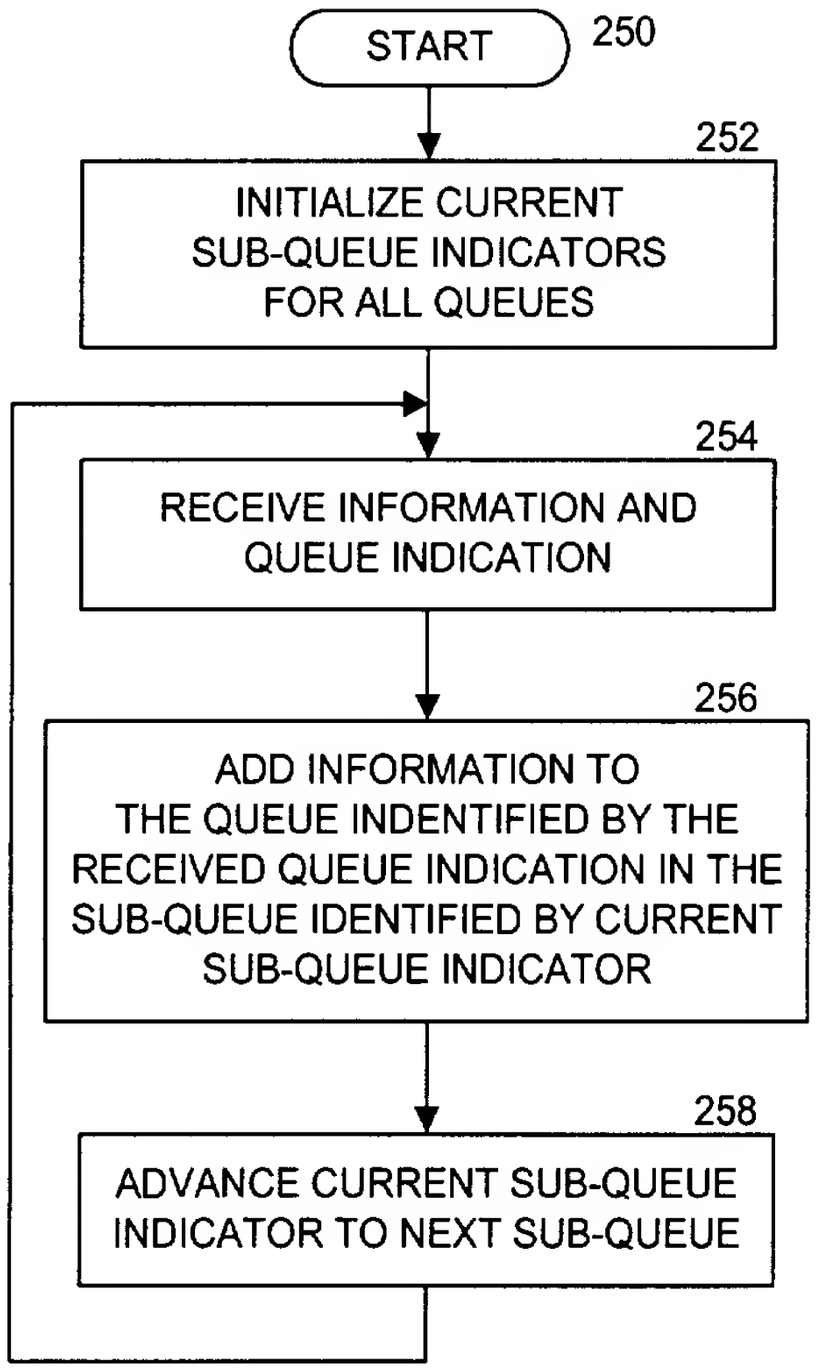

FIGURE 2B

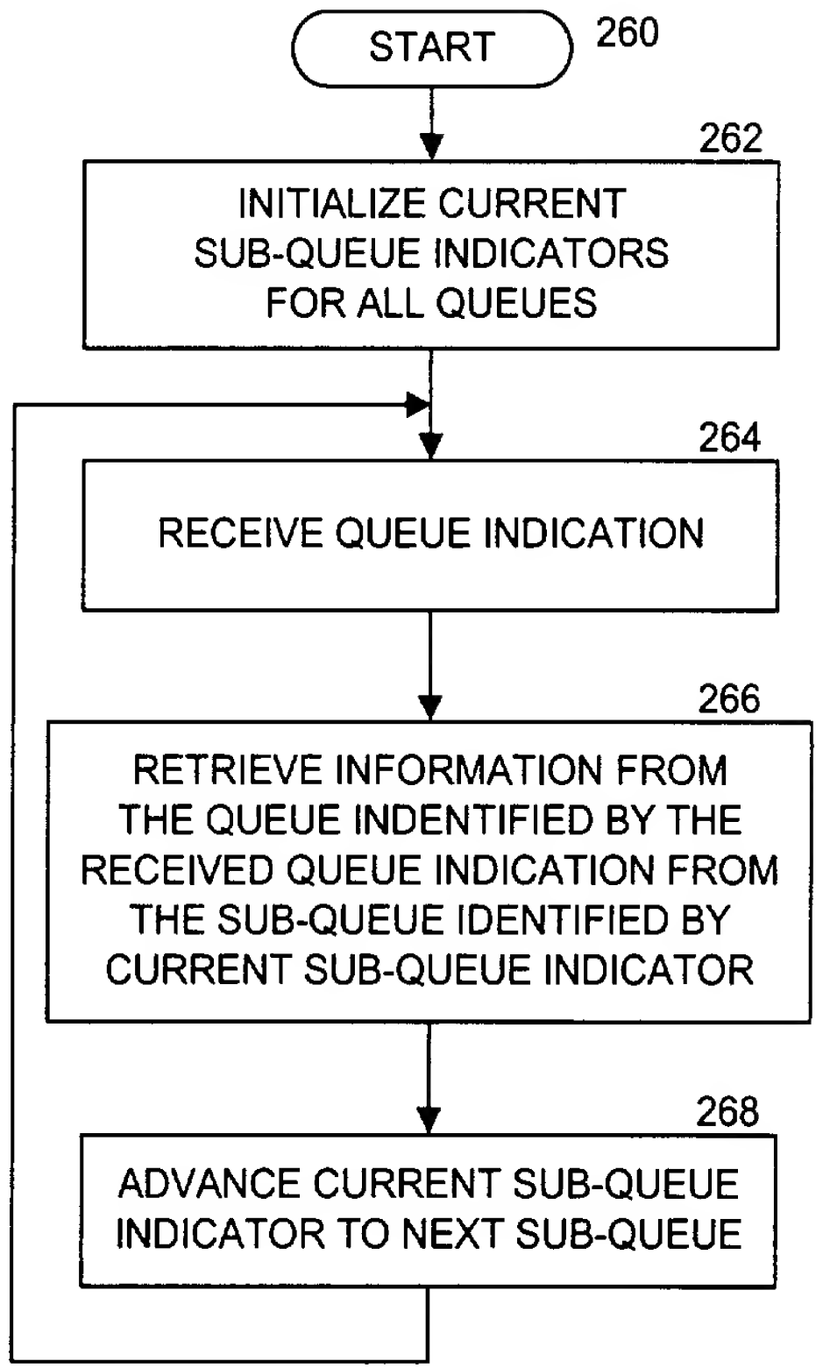

FIGURE 2C

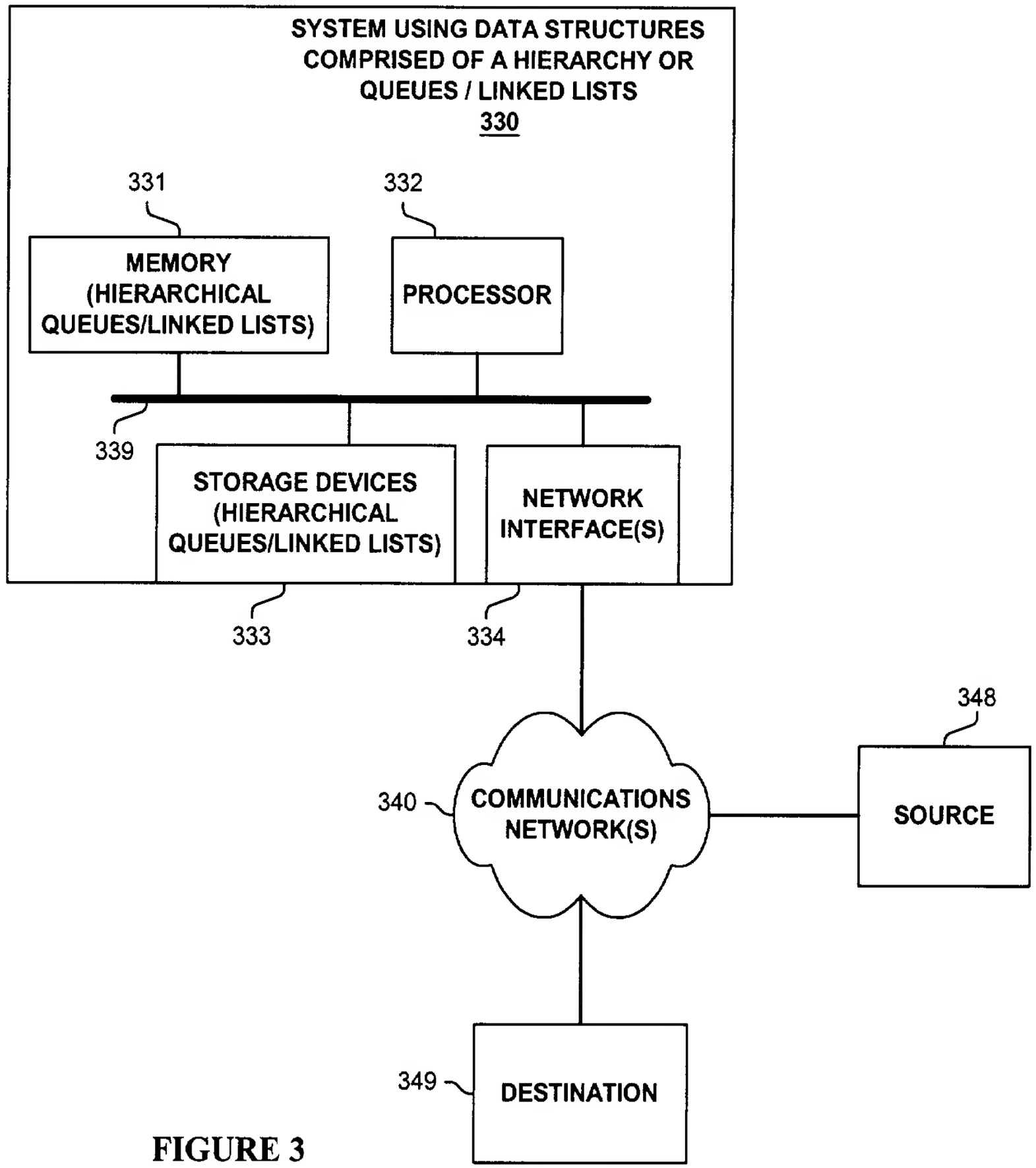
SYSTEM USING DATA STRUCTURES COMPRISED OF A HIERARCHY OR QUEUES / LINKED LISTS
330
331
MEMORY (HIERARCHICAL QUEUES/LINKED LISTS)
332
PROCESSOR
339
STORAGE DEVICES (HIERARCHICAL QUEUES/LINKED LISTS)
NETWORK INTERFACE(S)
333
334
348
340
COMMUNICATIONS NETWORK(S)
SOURCE
349
DESTINATION

FIGURE 3

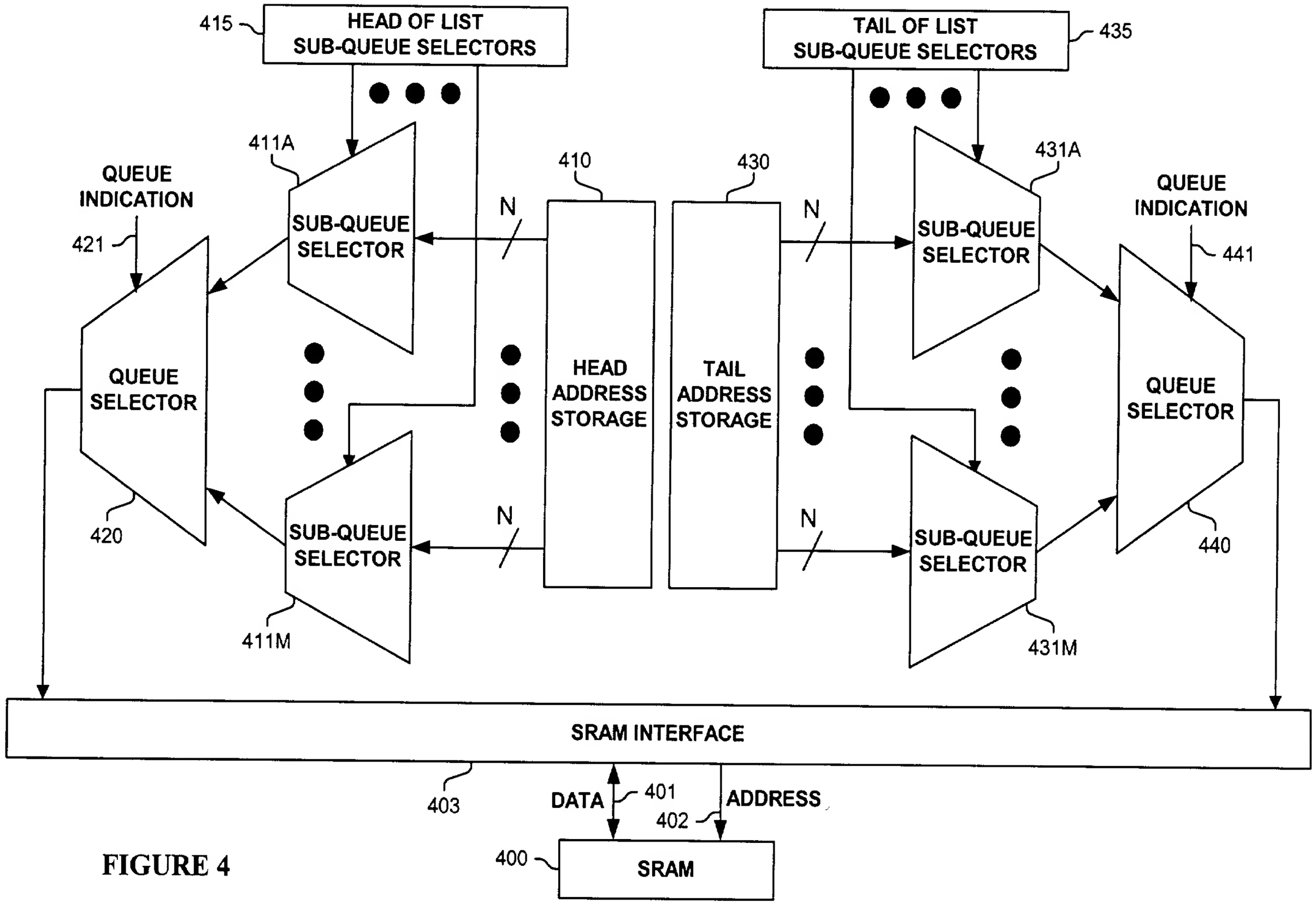
415
HEAD OF LIST
SUB-QUEUE SELECTORS
435
TAIL OF LIST
SUB-QUEUE SELECTORS
411A
410
430
431A
QUEUE
INDICATION
421
SUB-QUEUE
SELECTOR
N
N
SUB-QUEUE
SELECTOR
QUEUE
INDICATION
441
QUEUE
SELECTOR
HEAD
ADDRESS
STORAGE
TAIL
ADDRESS
STORAGE
QUEUE
SELECTOR
420
SUB-QUEUE
SELECTOR
N
N
SUB-QUEUE
SELECTOR
440
411M
431M
SRAM INTERFACE
403
DATA
401
ADDRESS
402
400
SRAM

FIGURE 4